Emulation and failure injection, a complement to Radiation Test

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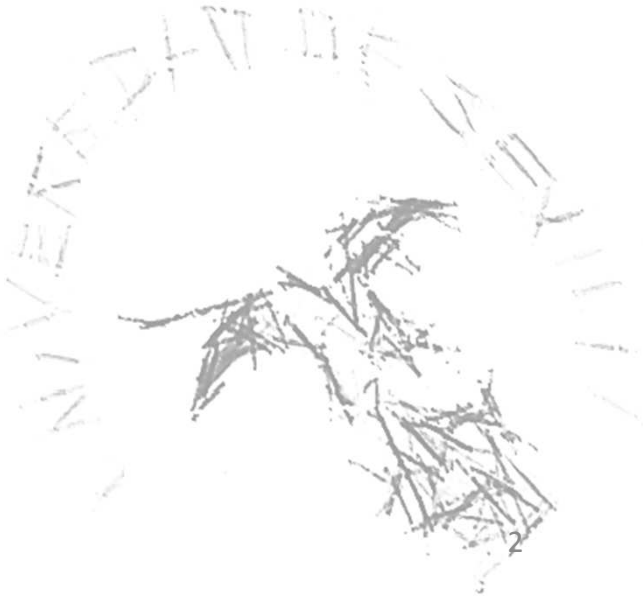
RADIATIONTEST WORKSHOP 2016
SEVILLE – SPAIN 31st MARCH – 1st APRIL

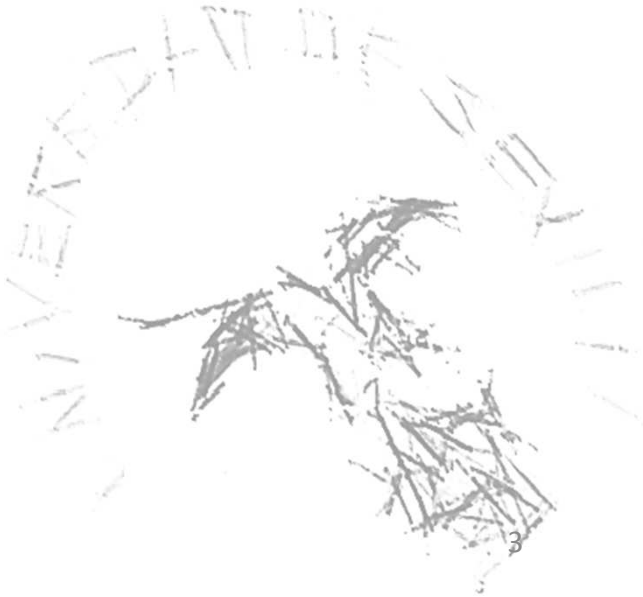
Motivation

- Single Event Test
- Radiation Test on complex devices requires in vivo testing
- Test Fixture is an important part of a test. It requires:
  - A good mitigation strategy for the DUT
  - A good stimuli set



Summary

I. Introduction
II. Norms and Guidances of Radiation Testing
III. Fault Injection. FT-UNSHADES2
IV. Contribution of FI to Radiation Testing
V. Conclusions
VI. Analog FTU

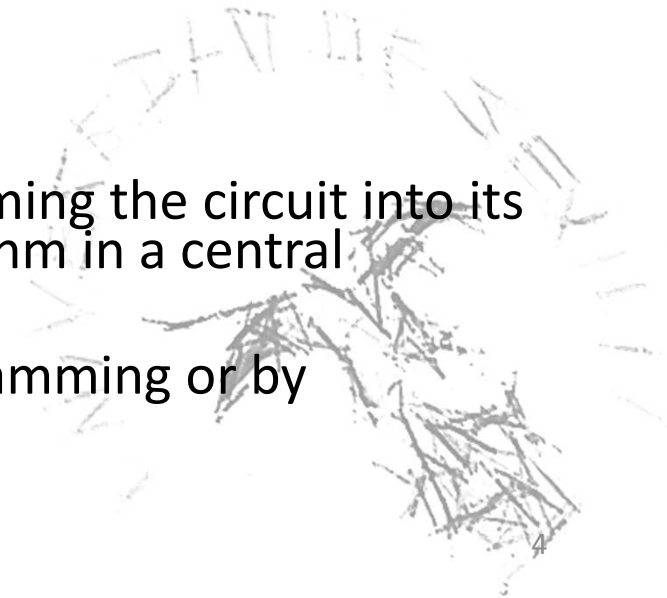


I. Introduction

- Soft Errors
  - Single Event Effects (SEU)
  - Multi Bit Effects (MBE)
  - Single Event Transient (SET)
  - Single Event Failure Interrupt (SEFI)
- Destructive Errors
  - Single Even Latch-up (SEL)
  - Single Even Bourn-out (SEB)
  - Single Event Gate Rupture (SEGR)

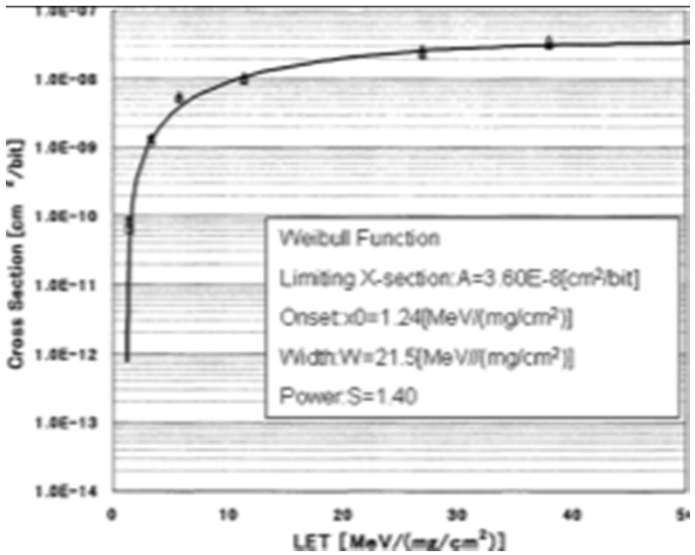
Soft errors – can be corrected by reprogramming the circuit into its correct logic state or by restarting the algorithm in a central processing unit

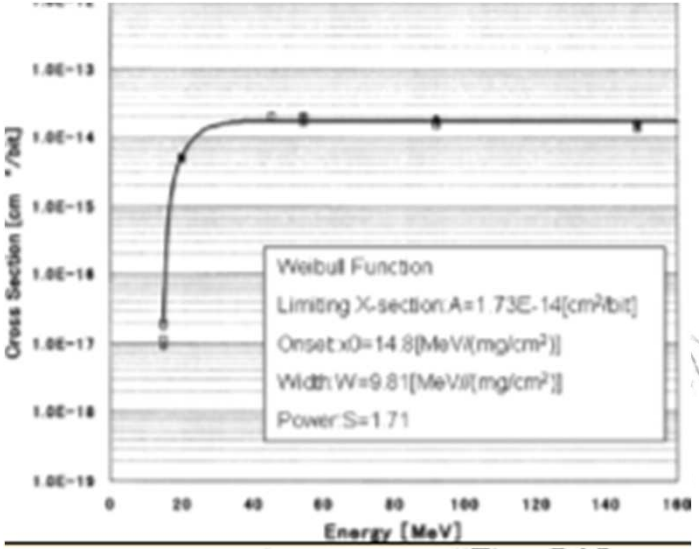
Hard errors – are not correctable by reprogramming or by restarting the algorithm



#Number of bit errors

Cross Section — $\sigma=N/\Phi$ — Fluence





Kimoto Y. et al., IEEE Trans. Nucl. Sci., vol. 52, pp. 1574–1578, Oct. 2005.

- Testing Complex VLSI Designs
- A test fixture is the necessary electronic arrangement to perform the test with the device stimulated:
  - Power limitators for protections against SEL
  - Temperature Measurement
  - Initialization policy
  - A method of measurement the collected errors
- A beam of heavy ions, protons or neutrons… using a particle accelerator
  - Known flux (particles/cm^2/s) and fluence (particles/cm^2)
  - Known energies or LET (Energy·cm^2/time)

II. Normatives and Guidelines of this Radiation Testing

USA:

- **EIA/JESD57:** Test procedures for the measurement of Single Event Effects in semiconductor devices from heavy ion irradiation;
- **ASTM F1192:** Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices;
- **MIL-STD-750 Method 1080:** Single-Event Burnout and Single-Event Gate Rupture.

Europe:

- **ESCC25100:** Single Event Effects Test Method and Guidelines
- **ECSS-Q-HB-60-02A DIR2**. Space Product Assurance. Techniques for radiation effects mitigation in ASICs and FPGAs handbook

Russia:

- **134-0175-2009:** Heavy-ion and proton induced SEE in digital circuits;
- **134-0191-2011:** Heavy-ion and proton induced SET in analog and mixed signal circuits;
- **134-0192-2011:** Heavy-ion and proton induced SEB and SEGR in power MOSFETs.

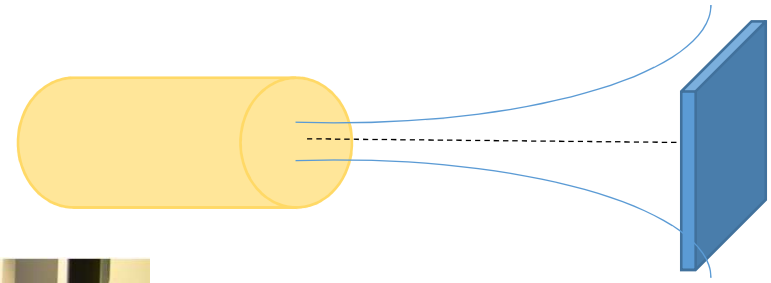
Poivey C., Buchner S., Howard J., LaBel K. Testing Guidelines for Single Event Transient (SET) Testing of Linear Devices. NASA-GSFC, 2003.

Buchner S., Marshall P., Kniffin S., LaBel K. Proton Test Guideline Development – Lessons Learned. NASA-GSFC, 2002.

Schwank J.R., Shaneyfelt M.R., Dodd P.E. Radiation Hardness Assurance Testing of Microelectronic Devices and Integrated Circuits: Radiation Environments, Physical Mechanisms, and Foundations for Hardness Assurance. Sandia National Laboratories Document SAND-2008-6851P.

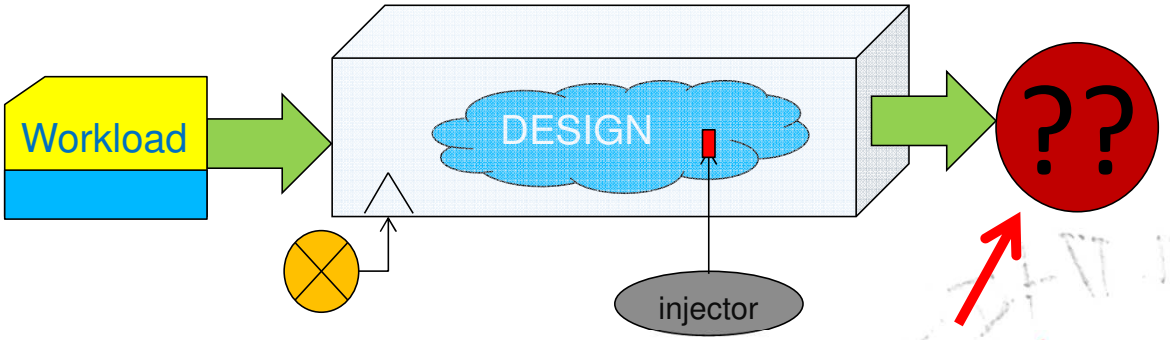
Schwank J.R., Shaneyfelt M.R., Dodd P.E. Radiation Hardness AssuranceTesting of Microelectronic Devices and Integrated Circuits: Test Guideline for Proton and Heavy Ion Single-Event Effects. Sandia National Laboratories Document SAND 2008-6983P.

- Test engineer vs Electronic Engineer

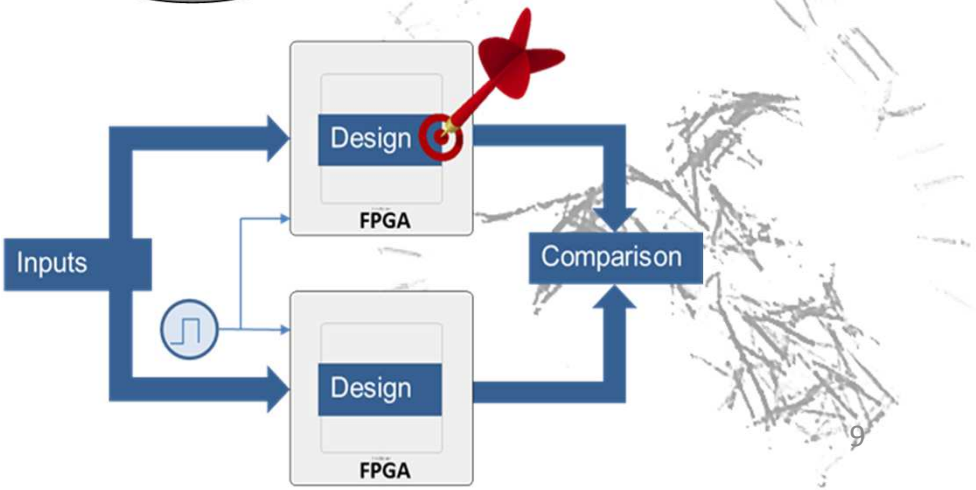


III. Principles of Fault Injection

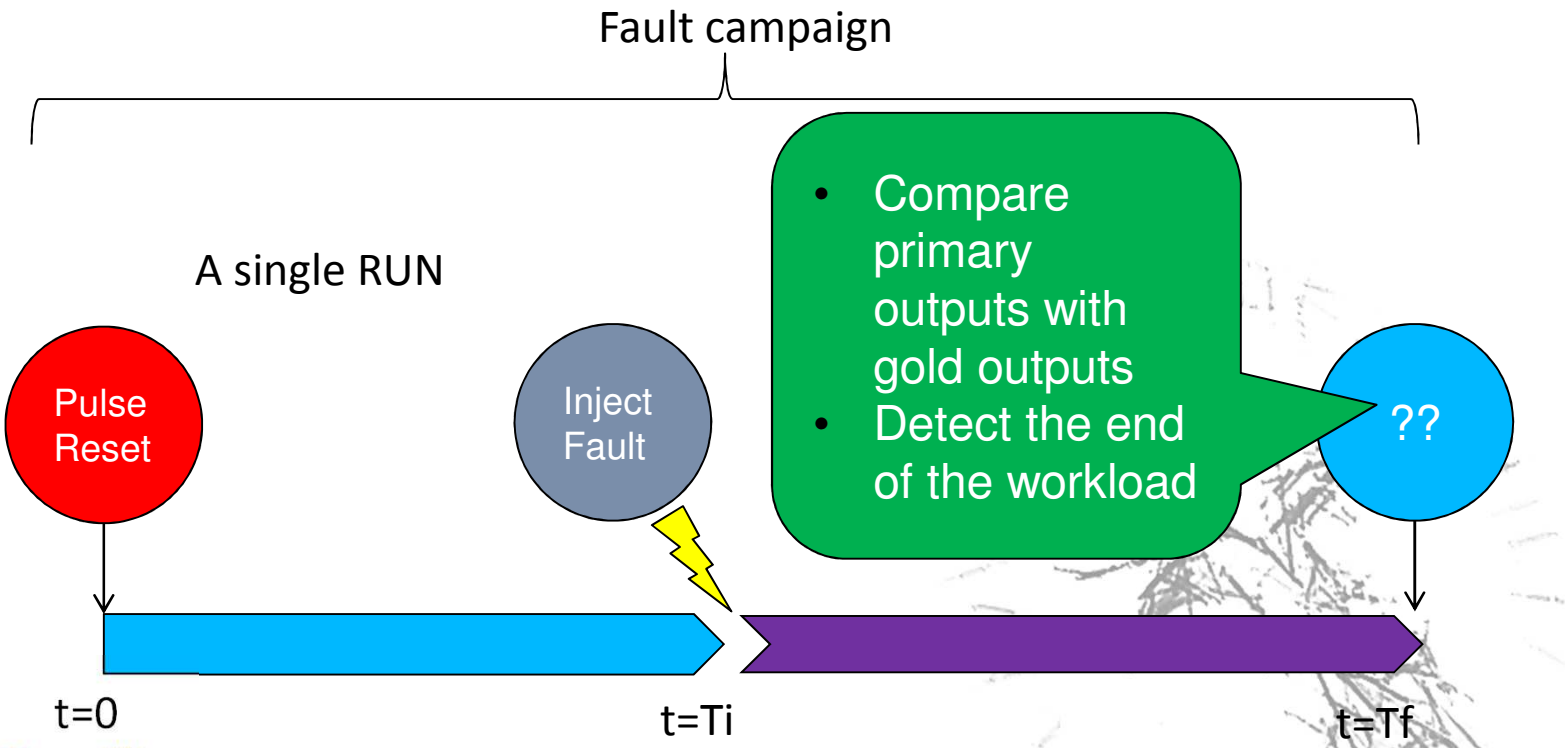
- Emulate the particle hitting using a controlled process in an FPGA as design support device.



FT-UNSHADES2



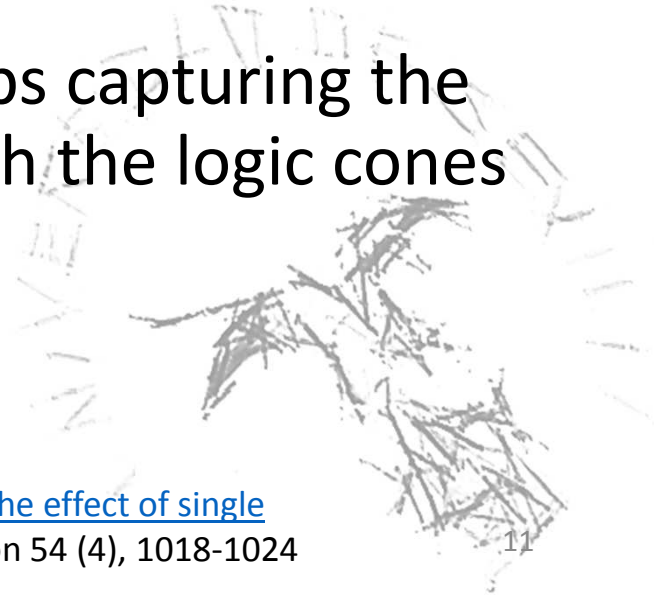
- The injected fault is a model of the physical effect under study.
- After an injection the result is recorded into a Fault Dictionary.
- The procedure is repeated a significant number of RUNS. This is called CAMPAIGN.



Fault models

REMARK: This mode of Fault Injection is done over the USER REGISTERS

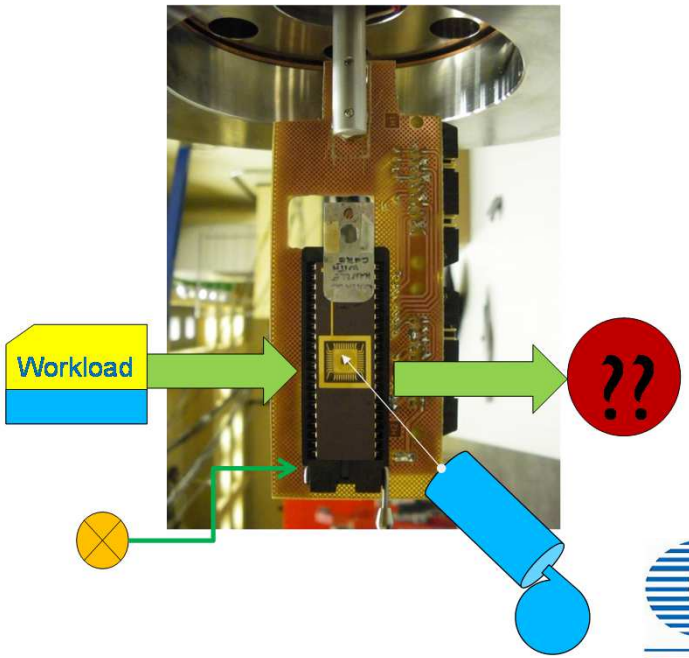
- SEU -> Simple bit flip
- MBU -> Several simultaneous bit flips paired by the layout
- SET -> Several simultaneous bit flips capturing the transient pulse propagated through the logic cones and captured by the registers.

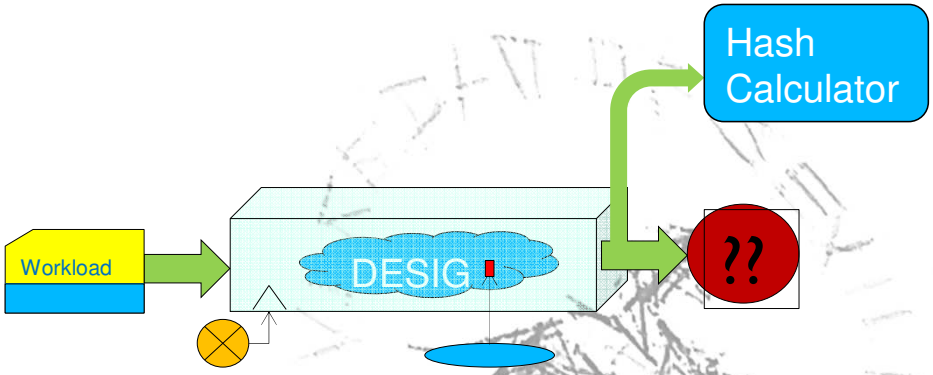


MA Aguirre, V Baena, J Tombs, M Violante A new approach to estimate the effect of single event transients in complex circuits Nuclear Science, IEEE Transactions on 54 (4), 1018-1024

Contributions of FI to Radiation Testing: Diagnostic

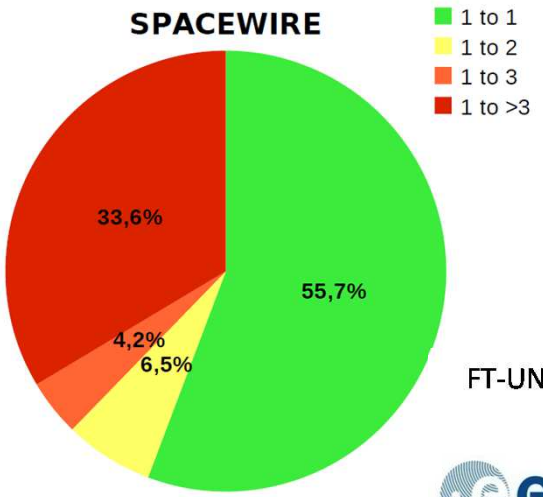
- The Workload can be improved using fault injection
- HASH codes are used to detect and diagnose faults



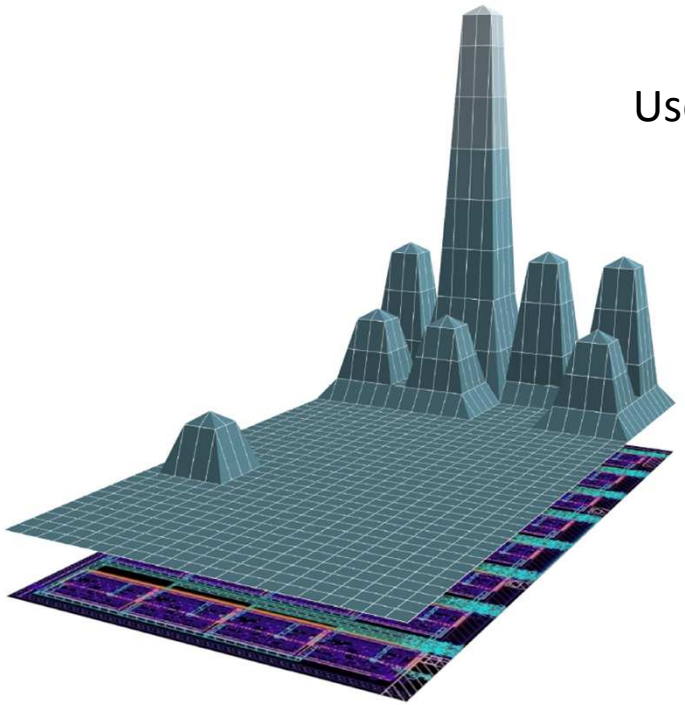


Centro Nacional de Aceleradores

- SpaceWire Codec IP core
  - **56% of errors are univocal**
  - 7% of errors have two candidates
  - 37% of errors have three or more candidates



FT-UNSHADES2



Use Microbeam facility at CNA

All the hitting particles were identified with their corresponding hash codes
This technique shows the utility of FI in the identification of beam test results.

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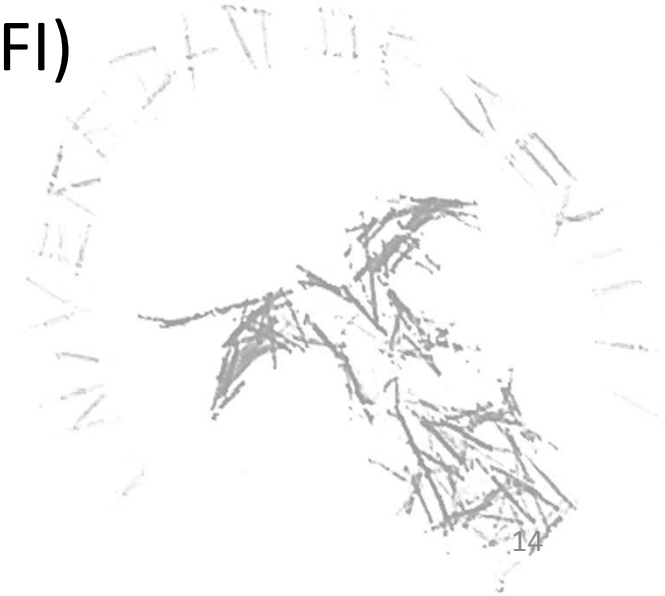
SRAM-FPGA Testing

There is a strong interest on SRAM-FPGAs in SPACE bussiness.

However it is a very sensitive device to SEE faults can hit in:

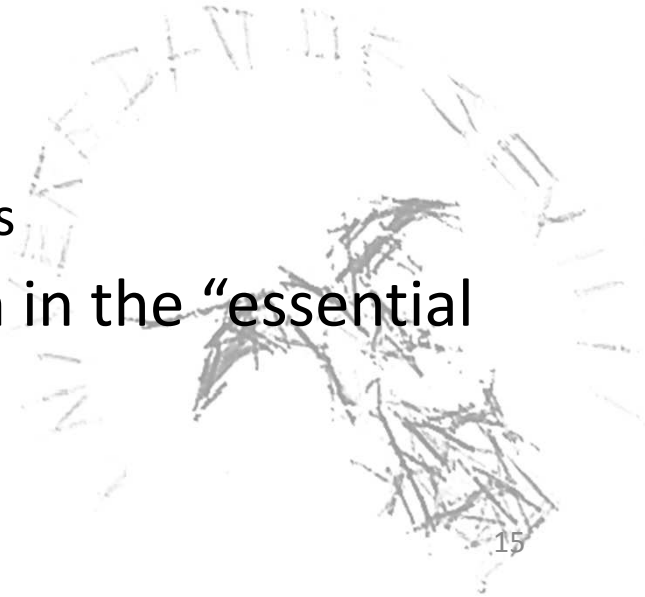
- Configuration memory (SEU and MBU)
- User registers (SEU)
- Configuration circuit (SEU, SEFI)



Faults on configuration memory

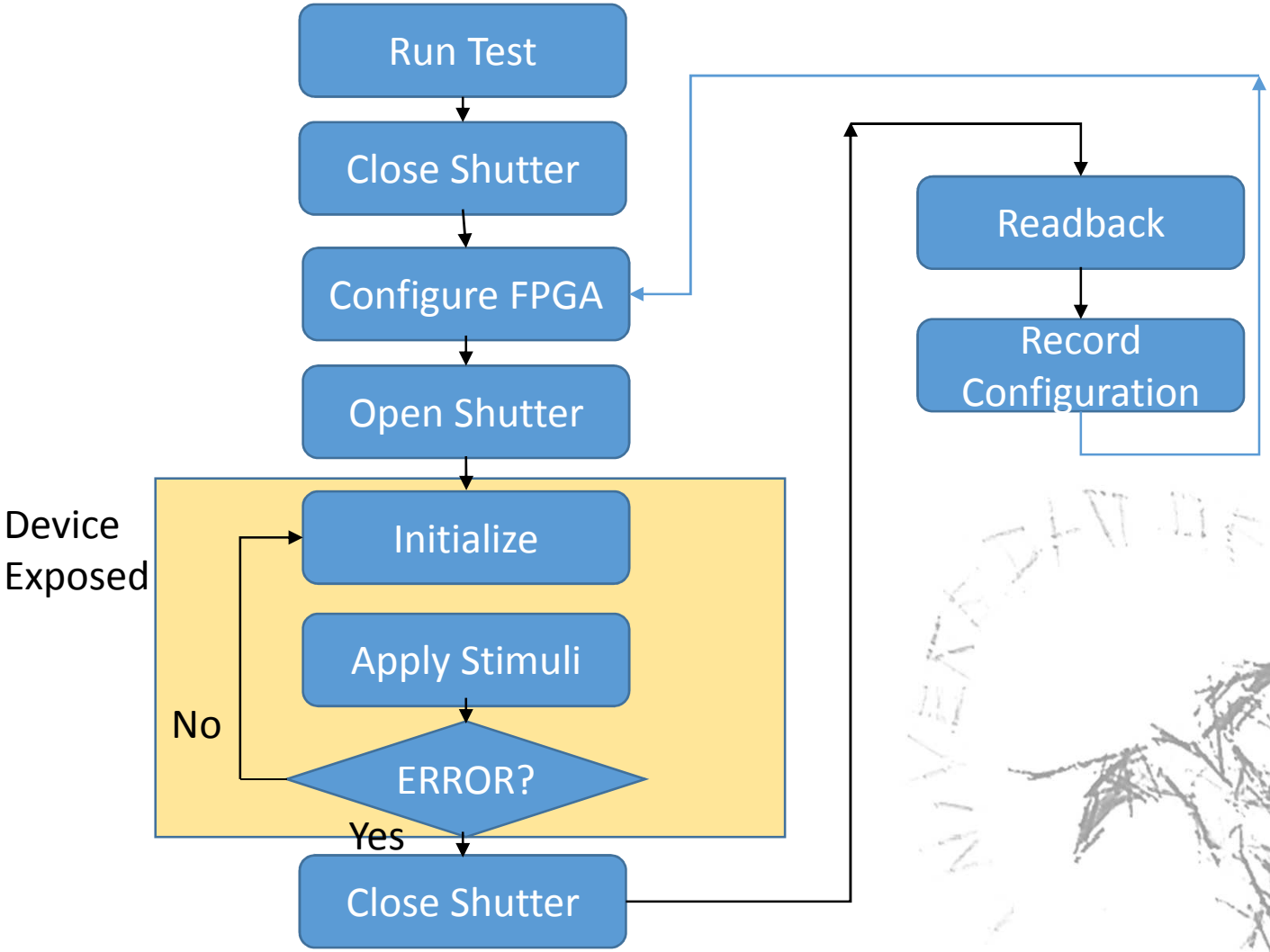
- Faults are permanent modification of the circuit
- Faults (in principle) do not propagate to other configuration memory cells
- Faults are related or unrelated to the configured circuit.
- Faults related
  - Produce an electrical influence
  - Critical -> Can be compensated by
  - Propagates to other configuration points

Xilinx produces part of this information in the “essential bits” file

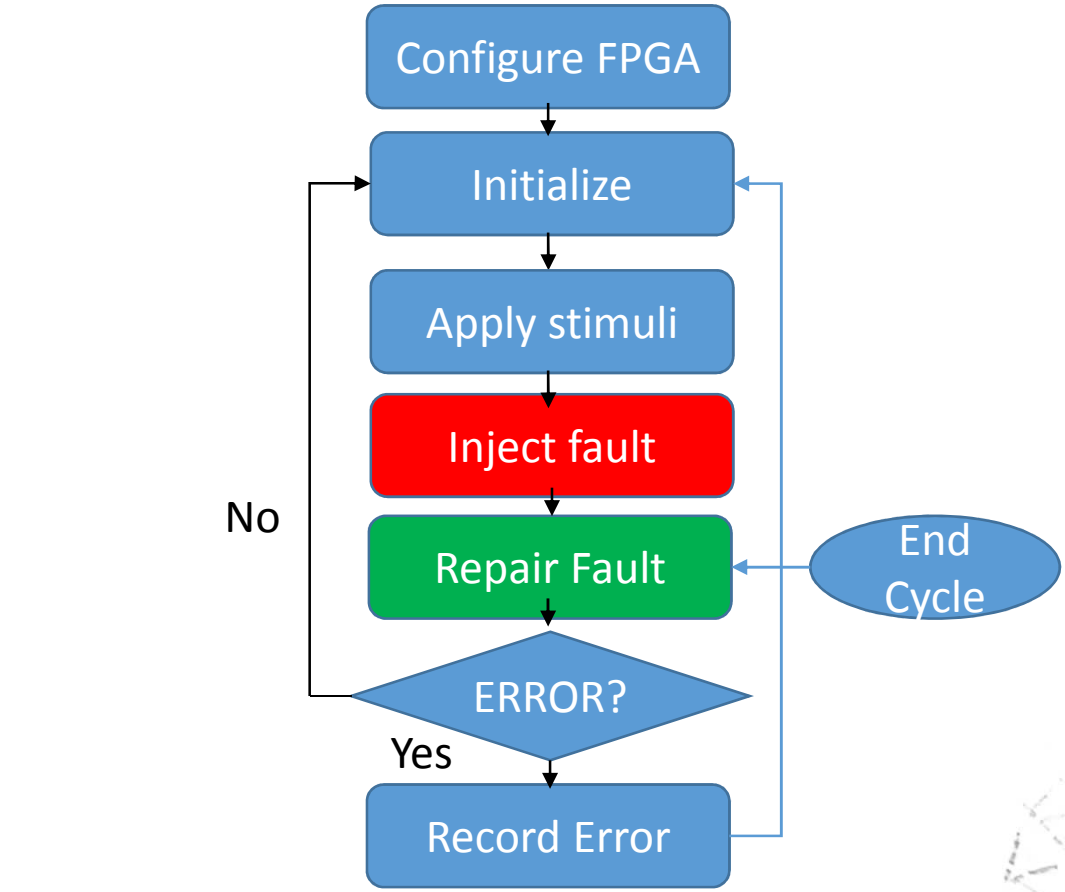


FPGA tests vs fault injection

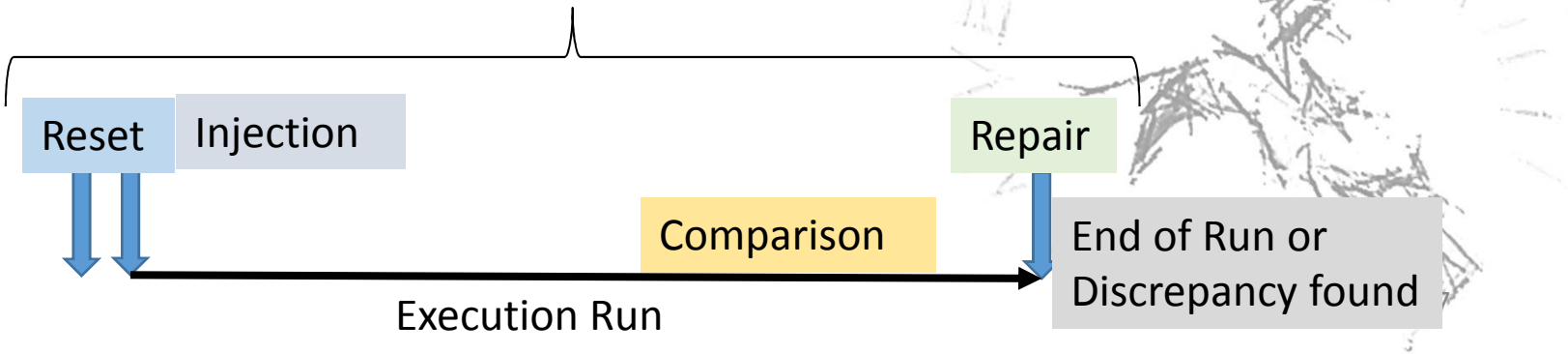
- Procedure for RADIATION testing in FPGAs



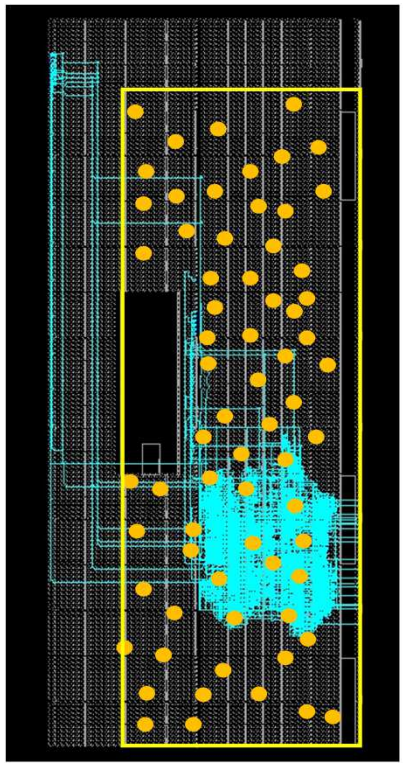
- Procedure for fault injection

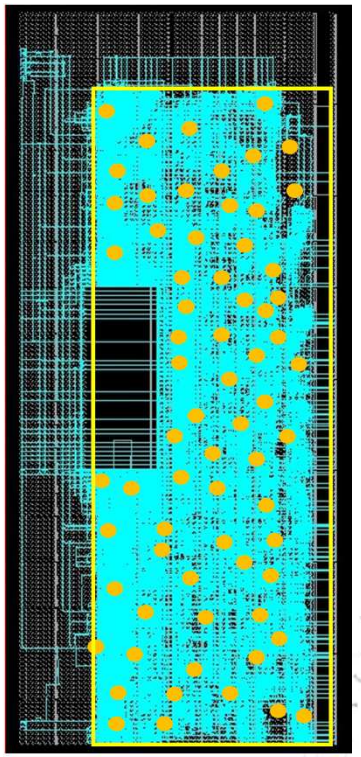


FT-UNSHADES2



- Random injection
- Repairing at the end of every cycle
- Comparison with same circuit irradiated in LANSCE



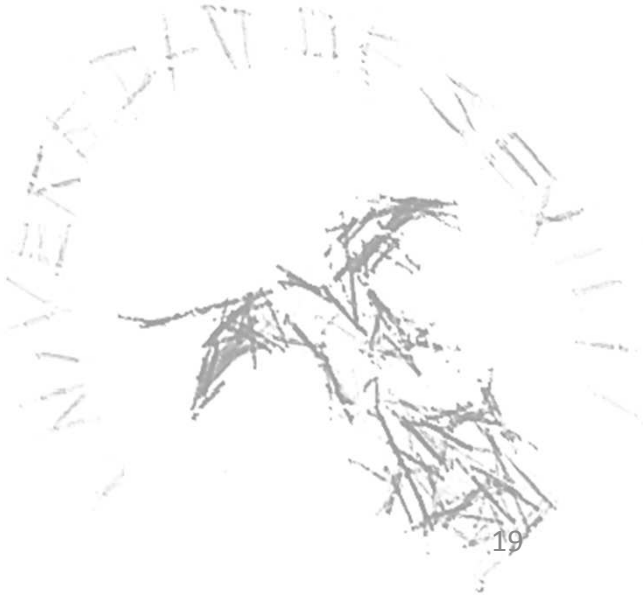


FT-UNSHADES2

- Preliminary results of injection over FX70T:

º	Faults Injected	Errors detected
B13_X30_plain	203.331	867
B13_X30_XTMR	203.326	469

Design and conditions	Device	Essential Bits	Total Essential Bits
B13_X30_plain (FTU2 circuit)	FX70T	333.525	18.936.096
B13_X30_XTMR (Polito circuit)	FX70T	1.912.920	18.936.096



V. Conclusions

- Fault injection is an useful technique to predict circuit behaviour under radiation
- A tool that produces prelimar results about the cross section of a design

FT-UNSHADES2 is a Fault Injection tool simple, ubiquotous and flexible

Easy to use with a strong learning curve

Accesible from Sevilla to any public institutions

Available for evaluation to companies

Thanks to Renaser, Renaser+ and Renaser3 national research projects, the Edelweiss regional research Project and ESA named FT-UNSHADES Project based on Xilinx.

The authors want to introduce the Brave FPGA through the VEGAS H2020 Project.

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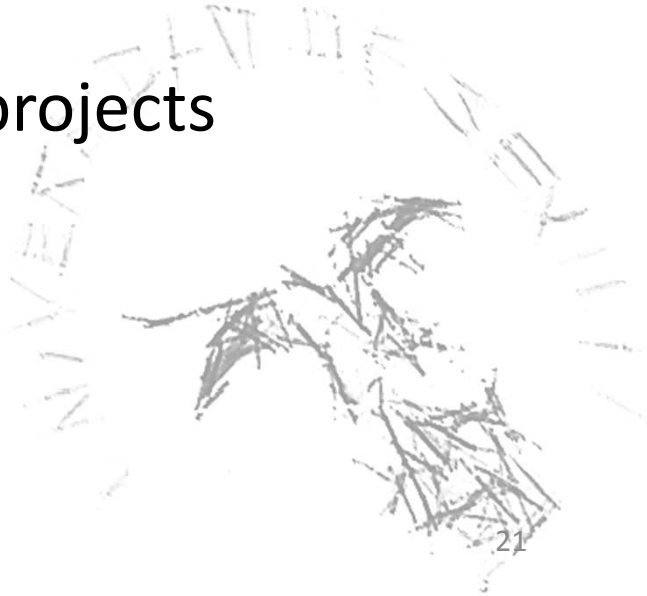
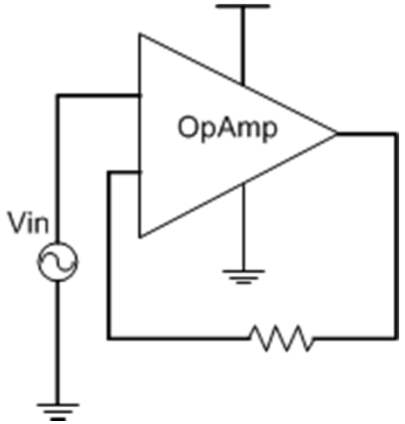
NANOXPLORE

VI. Analog FTU

- Fault injection using classical simulator
- Pluging of CADENCE tools.
- Used to predict critical points in the layout
- Automatic detection of certain layout vulnerabilities
- AFTU is used in several bussiness projects



- The analysis of several analog topologies has been performed:
  - Test-bench:



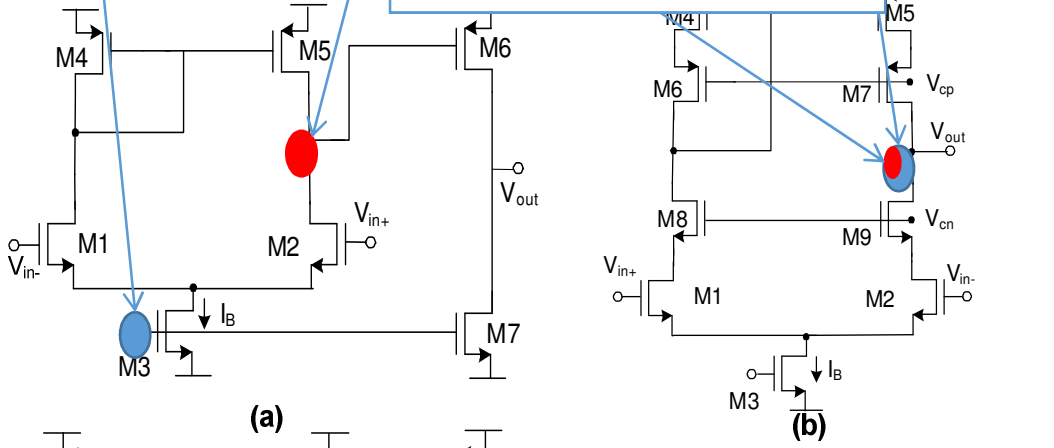
  - Input signal:
    - *A= 400mV*
    - *Fin= 200MHz (T=5ns)*

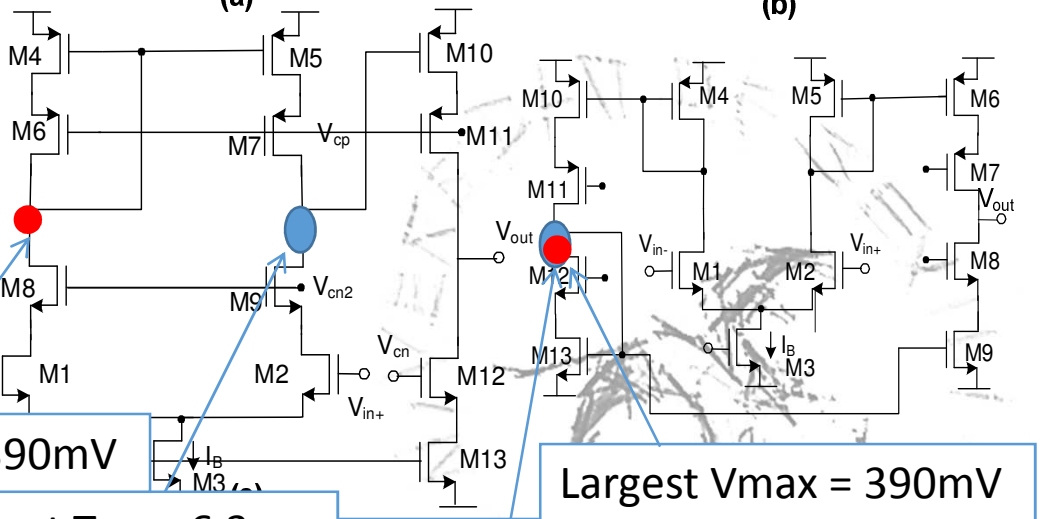
Longest Trec= 5.1ns

Largest Vmax = 290mV

Longest Trec= 4.4ns

Largest Vmax = 394mV





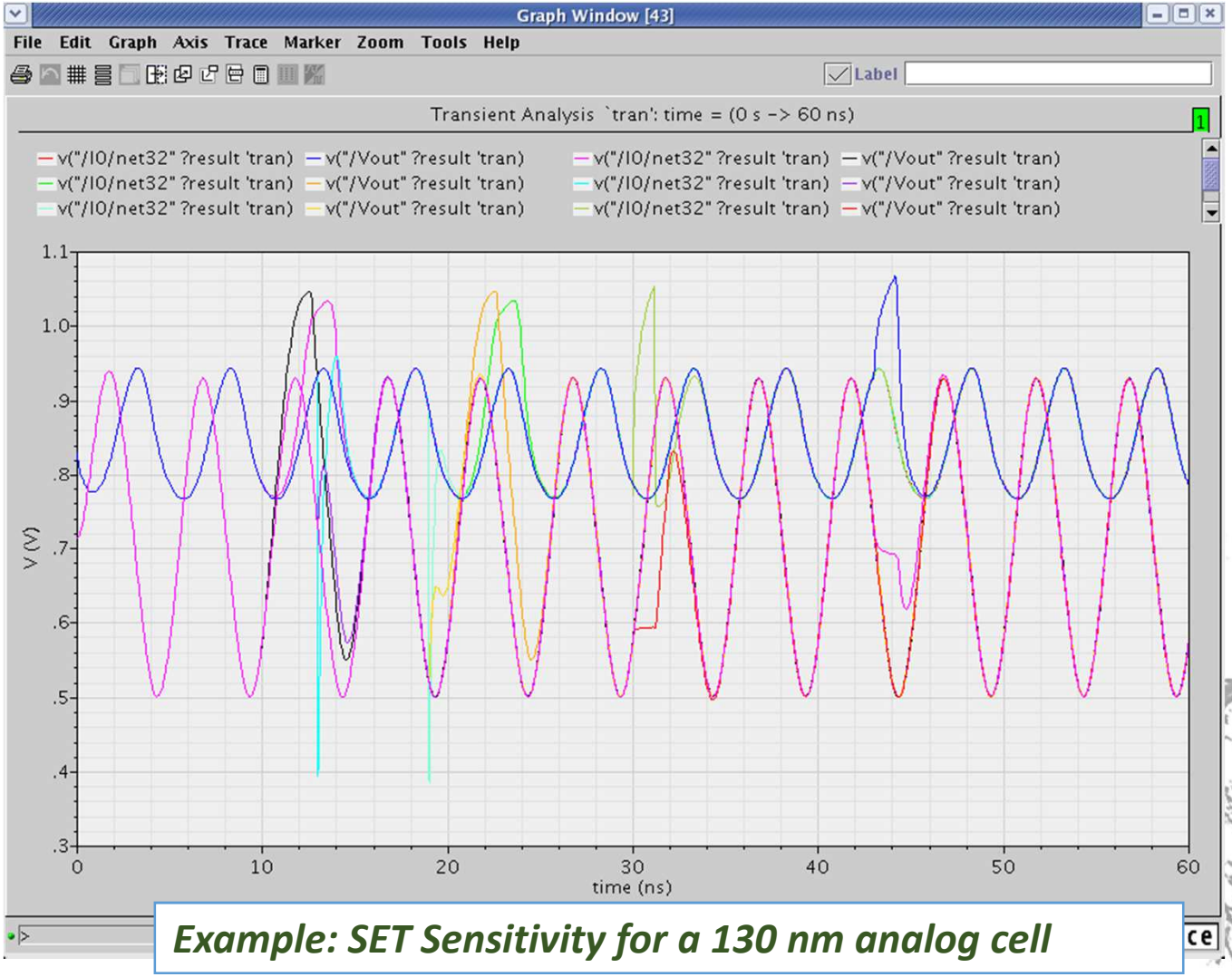
Largest Vmax = 390mV

Longest Trec= 6.3ns

Largest Vmax = 390mV

Longest Trec= 6.4ns

Example: SET Sensitivity for 130 nm analog cells



Example: SET Sensitivity for a 130 nm analog cell

Thank you…

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Questions?